ABSTRACT OF THE DISCLOSURE

A buffer circuit includes first and second transistors which are connected in series between first and second power supplies and which are controlled to be on/off based on values of signals at their control terminals are provided, in which a connection point between the two transistors is connected to an output terminal (OUT) and a control terminal of the first transistor is connected to an input terminal (IN), and a control circuit for performing on/off control over the second transistor based on an input signal from the input terminal (IN). The control circuit performs control so that when the input signal is at a second logic level corresponding to the second power supply, the second transistor is turned off, when the input signal goes to a first logic level corresponding to the first power supply, the second transistor is turned on to cause the output terminal (OUT) to a second power supply voltage, next, when the second transistor is turned off and then the input signal undergoes a transition from the first logic level to the second logic level and the first transistor switches from off to on, with the second transistor being kept off. A flip-flop is connected to the output terminal (OUT).